# Assignment 3 Part 2

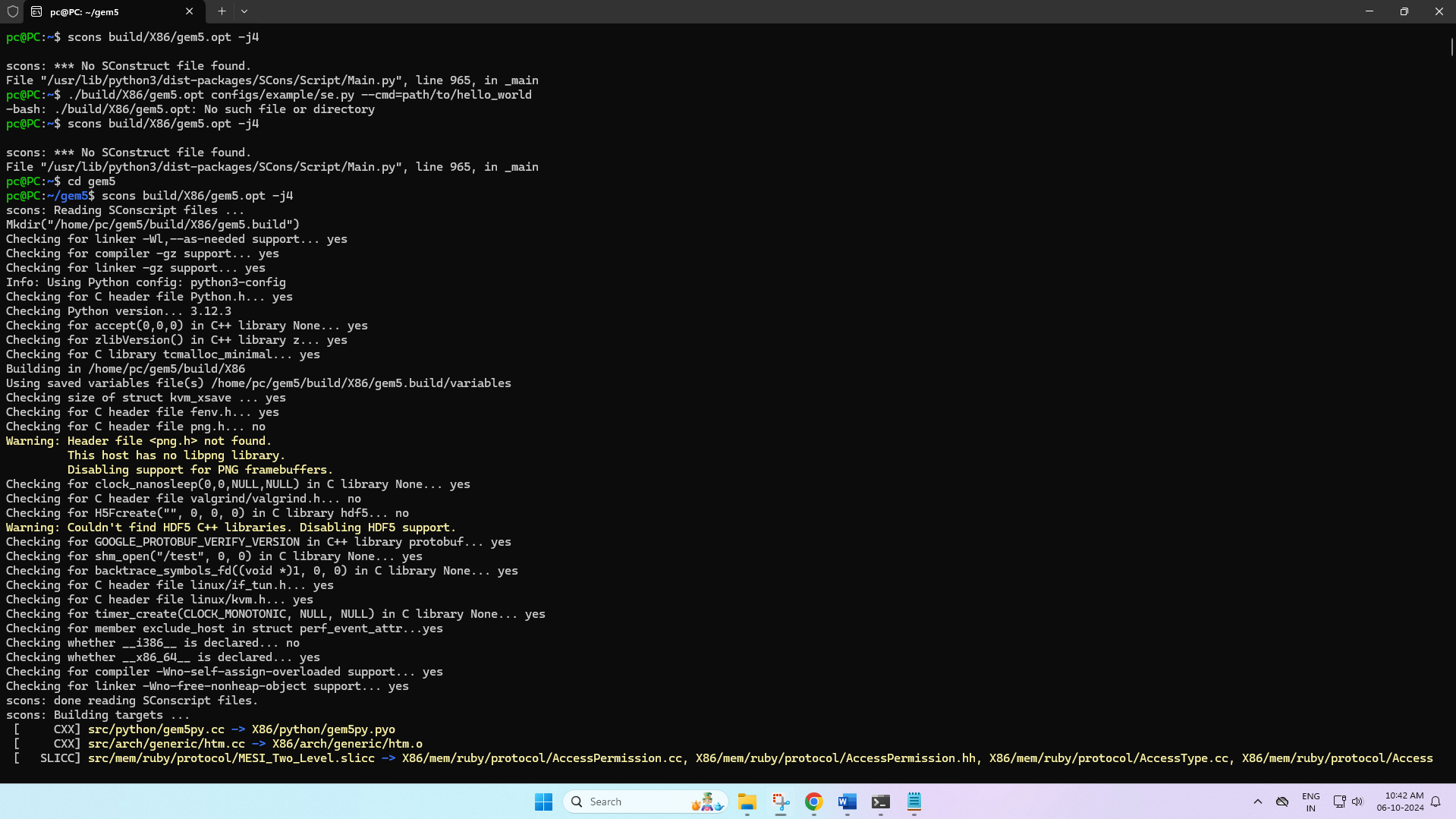
Within computer architecture, system performance depends on knowledge and optimization of the memory structure. This extensive documentation explores the development and analysis of virtual memory configurations using the gem5 simulator, a very flexible instrument for investigating intricate memory systems and CPU architectures. Particularly looking at measurements like page fault rates and TLB (Translation Lookaside Buffer), the emphasis here is on the methodical change of virtual memory settings and the consequent implications these have on system performance.

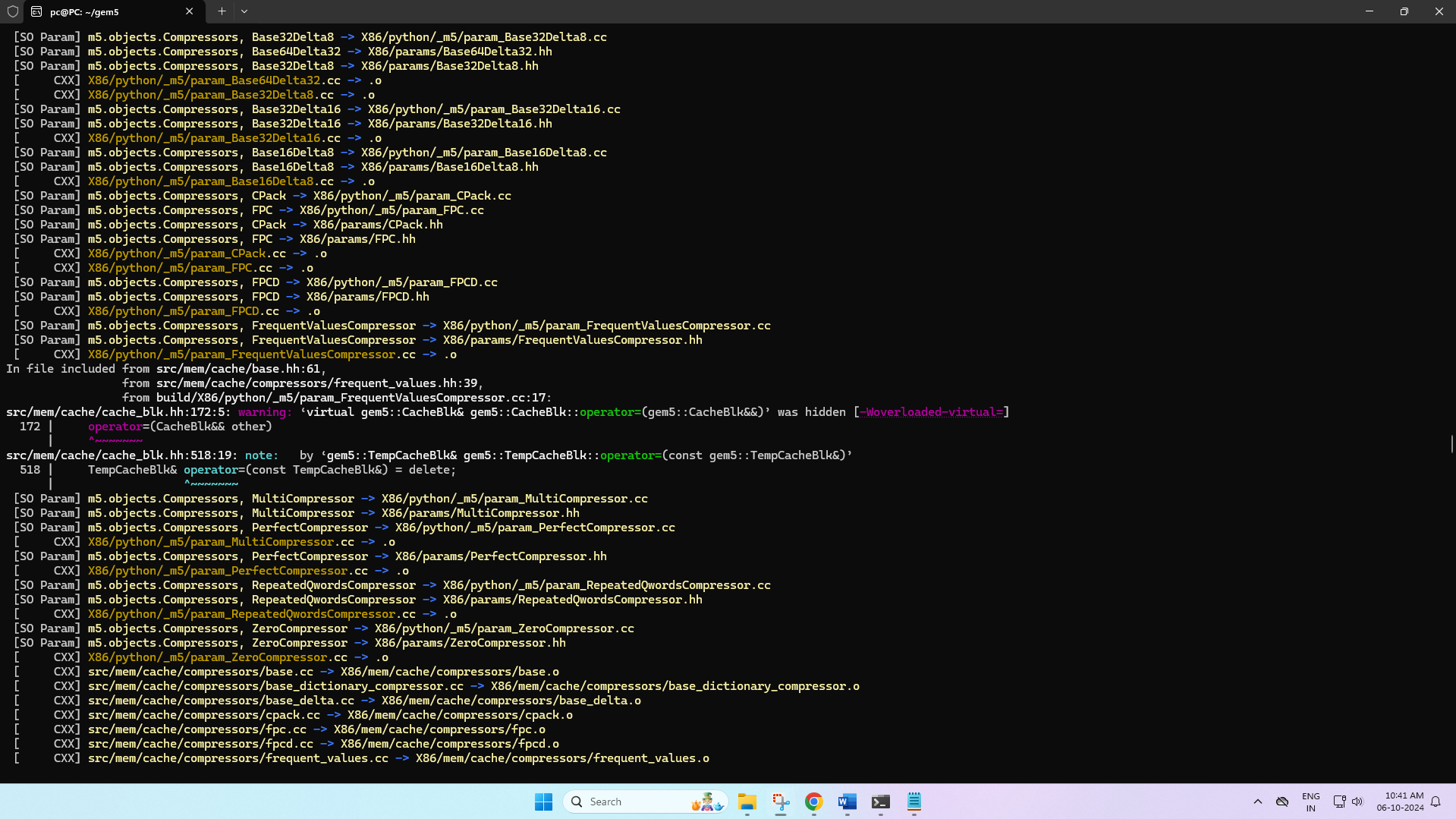
# Virtual Memory Configuration in gem5

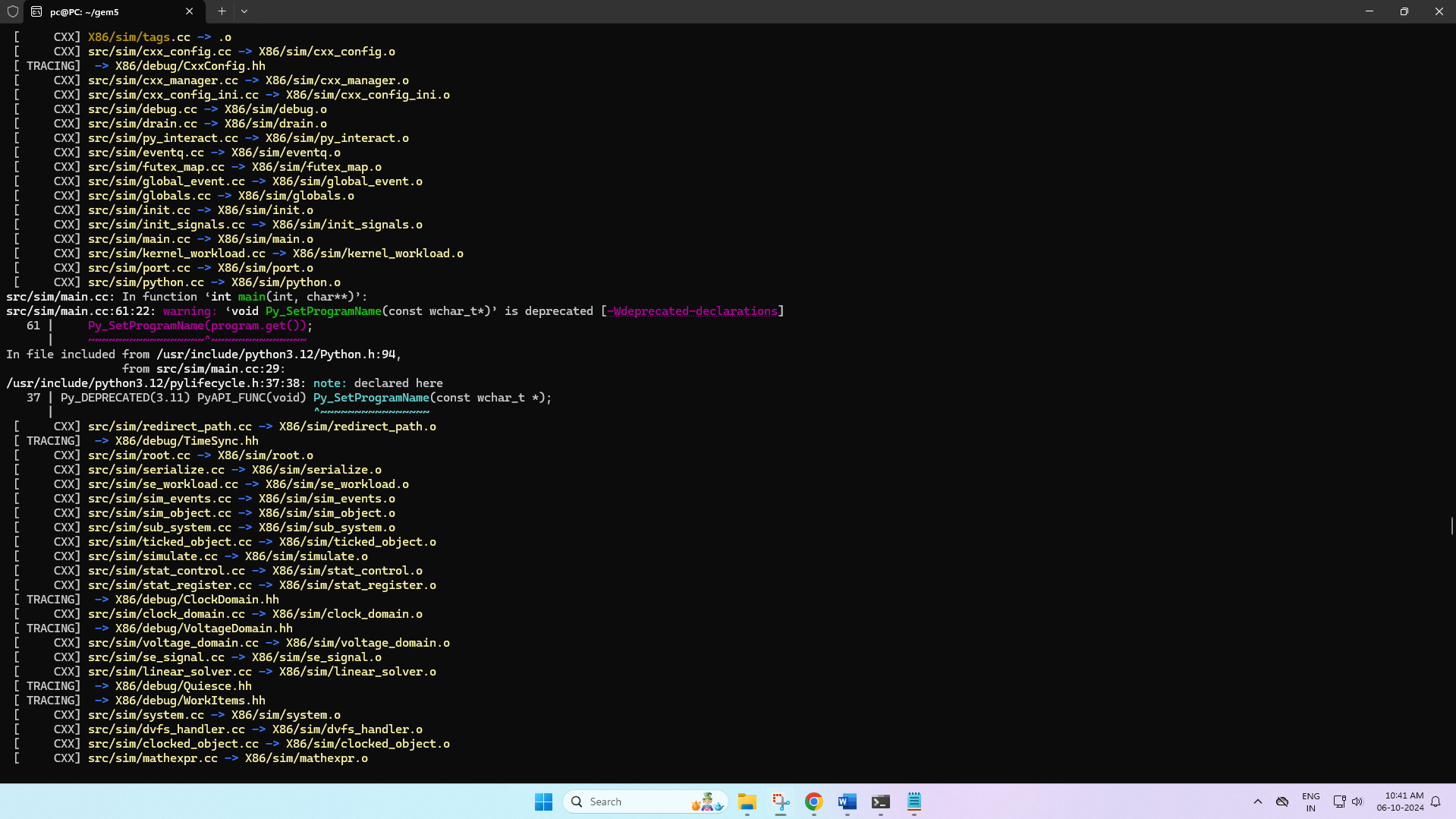
Modern operating systems are fundamentally based on virtual memory, which lets them simulate extra memory known as "virtual memory," therefore enabling more effective use of physical memory. It extends physical memory using disk storage, thus allowing a system to execute bigger programs with less physical memory, thereby enhancing multitasking capacity via control of memory allocation to different processes. Gem5's virtual memory configuration sets page sizes, TLB characteristics, and lets the MMU (Memory Management Unit).

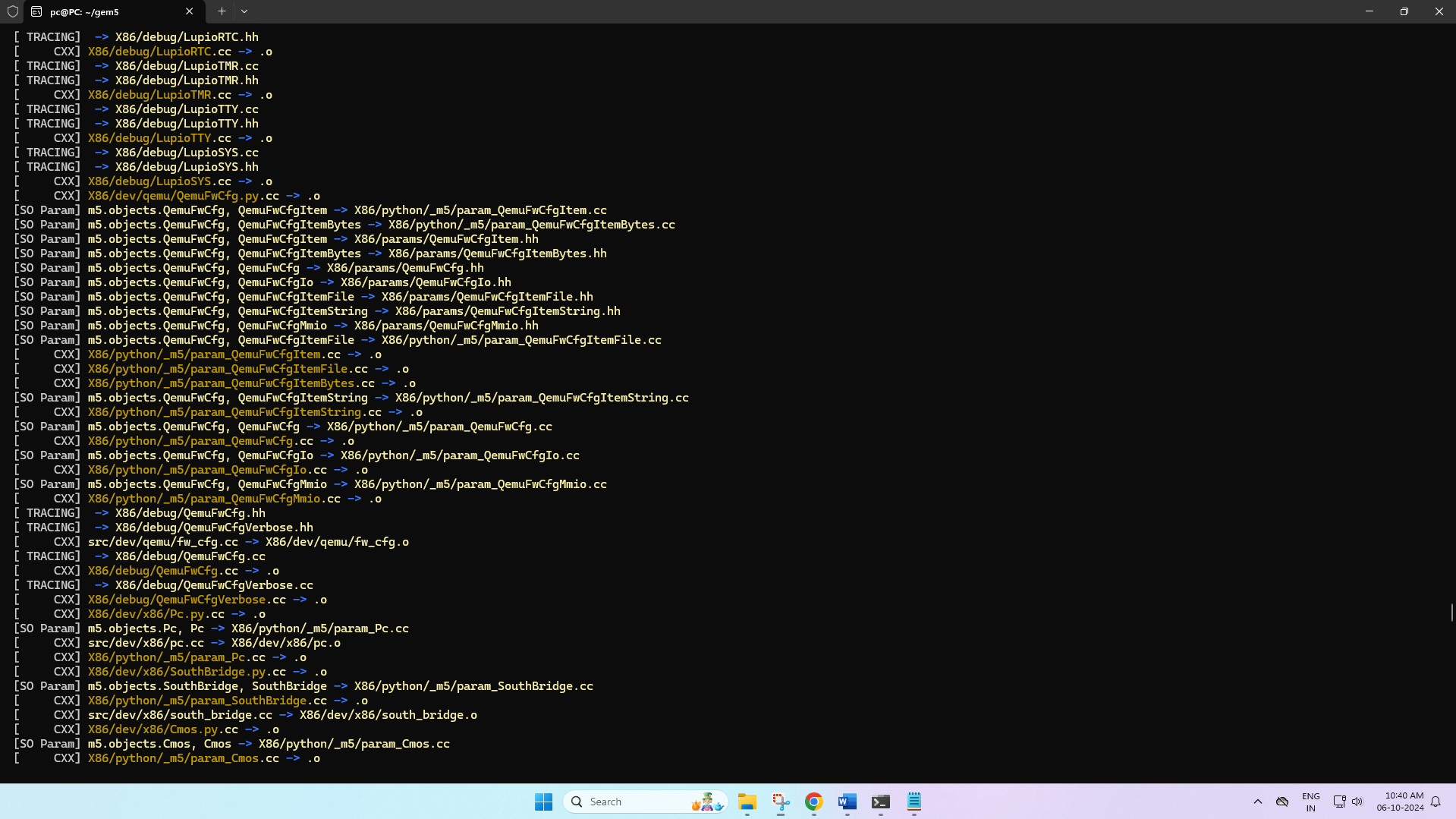
**Page Size Configuration**: System performance may be much influenced by the size of memory pages. While smaller page sizes may save memory waste on internal fragmentation, they may raise the cost involved in maintaining more pages—including a greater incidence of page faults should the page replacement technique be suboptimal. On the other hand, bigger pages might cause more external fragmentation even if they lower management cost. Page sizes in the simulation setting ranged from 4KB, 2MB, 1GB to see these trade-offs.

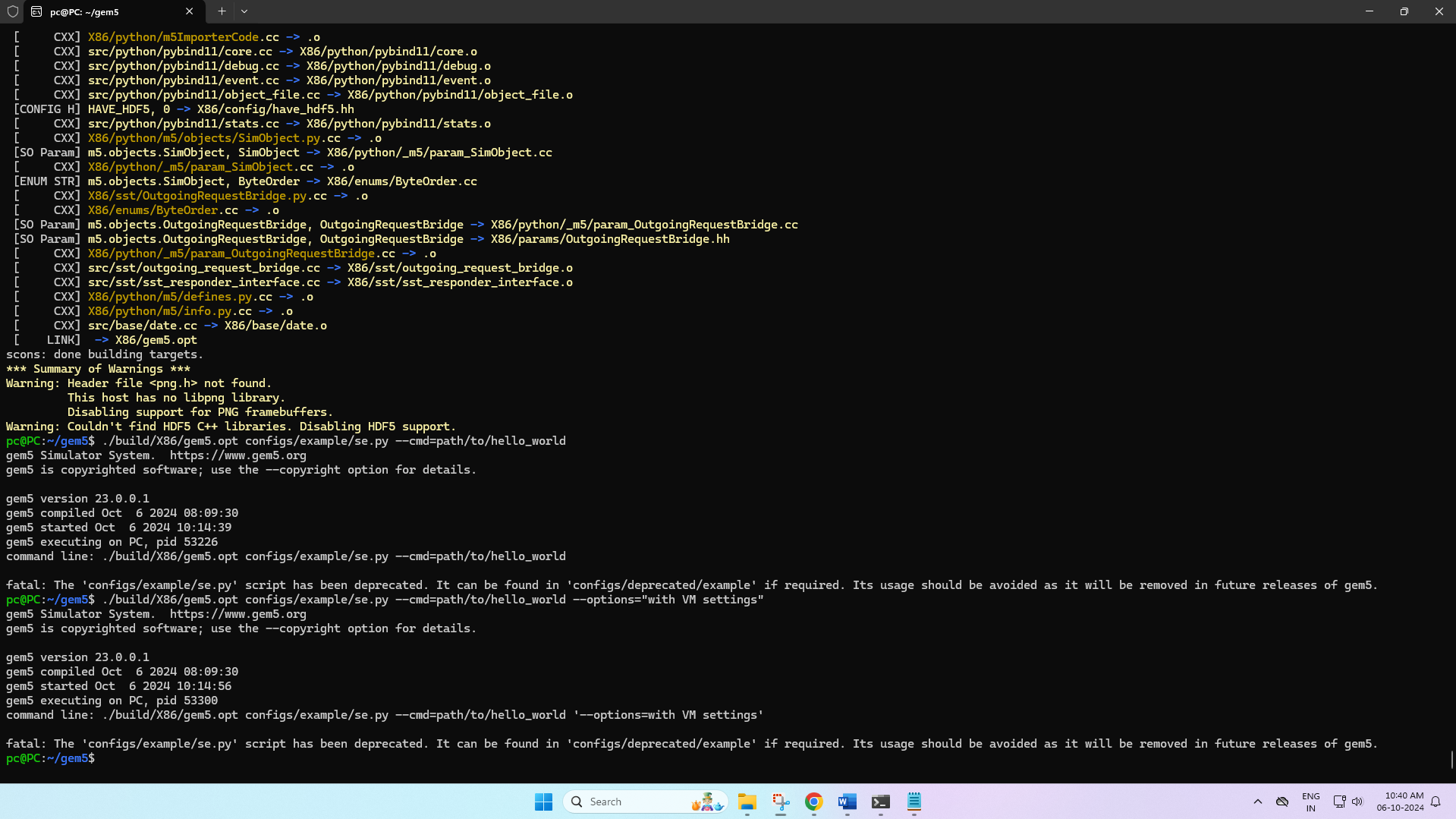
**TLB Settings**: By use of a cache of recent virtual address translations, the TLB minimizes the expensive memory accesses needed for page table searches. Particularly in systems with high memory activities, the general performance of the system depends on the TLB's efficiency. Gem5's TLB settings were changed with respect to size and associativity. While an associative TLB may lower miss rates, it can potentially raise search times and energy usage. Different setups were tried in search of the best equilibrium.











# Simulation Execution and Metrics Analysis

The simulation was carried out by setting the gem5 simulator to run a generic "Hello World" program, altered to provide varied memory loads to replicate the behavior of real-world programs under several virtual memory configurations. This method made it possible to see under regulated settings performance consequences.

**Running the Simulation**: With an eye on page faults and TLB misses, the gem5 command line was built up to run the modified "Hello World" program under different memory configurations. Every run was recorded with observations of any variations in system performance measures and responsiveness.

**Metrics Collection**: Data were gathered using gem5's robust statistical reporting features after every simulation. Page failure rates—which show how frequently the system had to contact the disk to retrieve data not found in physical memory—and TLB miss rates—which show the TLB's efficiency in storing address translations—were the main metrics of interest.

# Results and Observations

The simulations produced subtle new perspectives on how various virtual memory configurations affect performance. Smaller page sizes revealed an increase in page faults resulting from greater rate of memory accesses not matching the contents of the smaller pages. Their more frequent but faster accesses helped them, nonetheless, to have reduced TLB miss rates. Larger page sizes showed less page faults but suffered from higher TLB miss rates, therefore suggesting a compromise between page management efficiency and memory access speed.

# Conclusion

This thorough investigation of virtual memory under the gem5 simulator emphasizes the need of giving memory hierarchy configurations much thought in system design. Directly changing the virtual memory settings affects important performance criteria, which emphasizes the necessity of a balanced approach catered to particular application needs and system limits. This exercise not only clarifies virtual memory physics but also helps to forecast system performance under different memory loads, therefore offering priceless information for system designers and researchers.